REMARKS

Claims 1-22 were pending when last examined, all of which stand rejected.

The invention embodied in Claims 1-22 pertains to reconstruction of an IC package by electrically connecting a die to the lead frame of a pre-existing package and encapsulating the die. In the reconstruction process, lapping is used to shape the encapsulant of the new package.

While lapping is well known, it has heretofore not been applied for the purpose of encapsulant shaping, and especially for shaping an encapsulant in a reconstruction process. This invention is partially based on the discovery that lapping is well suited for encapsulant shaping in a chip reconstruction process because lapping is useful for both gross and precise removal of material.

Although the preamble of Claim 1 defines the scope of the inventive method as "reconstructing [of] an integrated circuit package," Claim 1 has been amended to emphasize this reconstruction aspect by explicitly reciting the deconstruction of the preexisting package.

Applicants respectfully request reconsideration of the claims in light of the above amendment and the following remarks.

Drawings

Drawings are objected to for failing to mention reference numerals 132 and 165 in the description. The specification has been amended to include the descriptions of these reference numerals.

The paragraph starting on page 22, line 30 has been amended to correct an obvious typographical error. The error is obvious because there is no "Block 103" in Figure 7B and "ultrasonic aluminum" is presented in block 132 in Figure 7B.

The paragraph starting on page 23, line 14 has been amended to explicitly state what is shown in Figures 8 and 9. The specification makes clear that the original IC package of the type disclosed in FIG. 1, FIG. 2, and FIG. 3 can be reconstructed, either with vertical walls (as in FIG. 4) or without vertical walls (as in FIG. 8). Since the IC packages of FIGs. 1, 2, and 3 include lead frames (25, 35, 45), a reconstruction of these IC packages also includes lead frames. The die attach pad 64 in FIG. 4 corresponds to the die attach pad 164 in FIG. 8, and the wire bonds 66 in FIG. 4 correspond to the wire bonds 166 in FIG. 8. Thus, the part labeled as reference numeral 165 in FIG. 8 corresponds to the lead frame 65 of FIG. 4.

An accompanying letter to the draftsperson addresses the issue of lines cutting through reference numerals.

Claim Rejections – 35 U.S.C. § 102

Claims 1-4 are rejected under 35 USC § 102(b) as being anticipated by U.S. Patent No. 6,080,602 to Tani et al. ("Tani").

Claim 1 is also patentable over Tani at least because it recites, "deconstructing an integrated circuit package for exposing a wire bond pad and a lead frame located therein ...." Unlike Tani's method, which pertains to *creating* chips by forming multiple subunits on a single substrate, the method of the invention pertains to *recycling* an existing IC package. Thus, Tani teaches depositing a resin material over multiple dice and then cutting the substrate to separate the dice. Tani does not disclose or suggest "deconstructing an integrated circuit package ..." as recited in Claim 1.

Claim 1 is patentable over Tani also because it recites that "at least a portion of the encapsulant reshaping is performed by a lapping process." Although the Examiner stated that Tani discloses using a lapping process, specifically citing Tani's col. 3, lines 28-37 and col. 4, lines 11-27, these cited sections do not disclose lapping. Col. 3, lines 28-37 discloses etching a lead frame pattern into a common substrate, and col. 4, lines 11-27 discloses using a dicing blade (54) to cut away a resin (52) for the purpose of flattening the surface, and mentions grinding as an alternative. As is well known, dicing and grinding are clearly distinguishable methods from lapping. Lapping, unlike dicing and grinding, affords greater control over the reshaping of the encapsulant.

Claim 1 is patentable over Tani for the above reasons. Claims 2-22, which depend from Claim 1, are patentable over Tani for at least the same reasons as Claim 1.

Claim Rejections – 35 USC § 103

Rejections over Tani and Iketani

As to Claims 5 and 6, which depend from Claim 1, they are deemed to be allowable for at least the same reasons Claim 1 is allowable. Applicants traverse the rejection under 35 USC § 103(a) over Tani in view of U.S. Patent No. 6,528,330 to Iketani ("Iketani") on the grounds that Tani and Iketani, even in combination, do not teach all the elements of Claims 5 and 6.

Claims 5 and 6, both of which depend from Claim 1, are patentable over a combination of Tani and Iketani for a number of other reasons. First, neither Tani nor Iketani teaches or suggests "deconstructing an integrated circuit package ...." Tani's and Iketani's methods pertain to *creating* chips by forming multiple subunits on a single substrate. In contrast, the method of the invention pertains to *recycling* an existing unit by deconstructing a pre-existing integrated circuit package and reconstructing the package with a new die. Second, neither Tani nor Iketani discloses "reshaping an upper surface of the encapsulant ... by a lapping process."

Additionally, Claim 6 is patentable over Tani and Iketani because it recites that "the reshaped upper surface of the encapsulant is sufficiently flat to permit labeling by printing, photolithographic or mechanical marking techniques...." As Iketani only mentions forming an indentation or printing a mark on the resin layer to indicate the polarity (Iketani, col. 10, lines 17-21), it is unclear whether Iketani's surface is "sufficiently flat to permit labeling."

Claims 5 and 6 are patentable over Tani and Iketani for the above reasons.

Rejections over Tani and Dlugokecki

Claims 7-11, 13-17, and 21 are rejected under 35 USC § 103(a) as being unpatentable over Tani in view of U.S. Patent No. 5,406,117 to Dlugokecki et al. ("Dlugokecki").

Claims 7-11, 13-17, and 21 depend from Claim 1, and are patentable over a combination of Tani and Dlugokecki because they recite, "deconstructing an integrated circuit package for exposing a wire bond pad and a lead frame located therein." As stated above, the method of the subject invention concerns recycling, not creating, a chip. Dlugokecki, like Tani, does not teach or even suggest deconstructing an intergrated circuit package.

Furthermore, Claims 7-11, 13-17, and 21 are patentable over Tani and Dlugokecki because they recite, "reshaping an upper surface of the encapsulant ... by a lapping process." As explained above in reference to Claims 1-4, Tani does not teach or suggest using lapping.

Rejections over Tani and Wensink

Claims 12, 18-20, and 22 are rejected under 35 USC § 103(a) as being unpatentable over Tani in view of U.S. Patent No. 4,384,917 to Wensink ("Wensink").

Claims 12, 18-20, and 22 depend from Claim 1 and are patentable over a combination of Tani and Wensink at least because they recite, "deconstructing an integrated circuit package for

exposing a wire bond pad and a lead frame located therein," and "reshaping an upper surface of the encapsulant ... by a lapping process." As mentioned above, Tani does not disclose deconstructing an integrated circuit package because Tani concerns with creating a new chip rather than recyling a preexisting chip. Furthermore, Tani does not disclose using lapping. As for Wensink, it does not disclose deconstructing an IC package because the focus of Wensink's teaching is material removal by etching. Since Wensink uses an etchant, there is no teaching or suggestion of using lapping.

For the above reasons, Claims 12, 18-20, and 22 are patentable over Tani and Wensink.

Conclusion

Applicants requests reconsideration of Claims 1-22 in light of the above amendments and remarks. If the Examiner wishes to discuss any aspect of this application, the Examiner is invited to telephone Applicants' undersigned attorney at 650-833-2121.

Any fee due for this Amendment may be charged to Deposit Account No. 07-1896.

Respectfully submitted,

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